Remarks

In view of the above amendments and the following remarks, reconsideration of the rejection and further examination are requested.

Claims 3-6 have been rejected under 35 U.S.C. §102(b) as being anticipated by Akerib (US 5,974,521).

Claim 3 has been amended so as to further distinguish the present invention from the reference relied upon in the rejection. Further, new claim 7 has been added.

It is submitted that the above-mentioned rejection is no longer applicable to the amended claims for the following reasons.

Claim 3 is patentable over Akerib, since claim 3 recites an image processor including, in part: a first storage unit operable to store separated image data formed by several pieces of pixel data, the separated image data having a predetermined width and being separated from lines of image data; a filtering unit operable to filter target pixel data subject to filtering using predetermined pieces of the pixel data, thereby outputting filtered pixel data and non-filtered pixel data, the predetermined pieces of the pixel data including the target pixel data subject to filtering and non-target pixel data subject to filtering; a setting unit operable to set a mode signal indicating whether or not the non-filtered pixel data is to be fed; and a data output control unit operable to control feeding of the non-filtered pixel data according to the mode signal, wherein the first storage unit has a same width as the predetermined width, the lines of image data have a same width as a line of display, and the non-filtered pixel data is generated by the non-target pixel data subject to filtering. Akerib fails to disclose or suggest these features of claim 3.

Akerib discloses a signal processing apparatus including a simultaneously accessible FIFO 10, a processor element array 16, a data link 30, and a controller 40. The processor element array 16 includes a plurality of processor elements (PEs) 20 that are controlled by the controller 40. The FIFO 10 receives and stores at least a portion of an incoming signal (e.g., an image) and feeds subportions of the signal to the PEs 20 in the processor element array 16. Each PE 20 processes the respective subportion of the image and includes at least one associative memory cell for storing the subportion of the image. The PEs 20 then output the processed subportions to the data link 30. (See column 13, line 55 – column 15, line 49 and Figure 1).

In the rejection, the FIFO 10 is relied upon as disclosing a portion of the operations performed by the claimed filtering unit. More specifically, the rejection indicates that the image

I/O mode of the FIFO 10 corresponds to the output of non-filtered pixel data and the image exchange mode corresponds to the output of filtered pixel data. However, such a comparison is without merit.

The claimed filtering unit is operable to filter target pixel data subject to filtering by using predetermined pieces of pixel data and output filtered pixel data and non-filtered pixel data. Further, the predetermined pieces of pixel data are recited as including the target pixel data subject to filtering and non-target pixel data subject to filtering, and the non-filtered pixel data is generated by the non-target pixel data subject to filtering. On the other hand, in the image I/O mode of the FIFO 10, a new image is read into the FIFO 10, while the processed (proceeding) image is written out. (See column 21, line 31 – column 22, line 21). There is no disclosure or suggestion of performing filtering as recited with respect to the claimed filtering unit in the discussion of the operation of the FIFO 10 in Akerib.

Further, the rejection also relies on the general discussion in Akerib of the use of filters at column 35, lines 42-54 as disclosing the remainder of the operations of the claimed filtering unit. However, it is clear that this mention of filtering in Akerib also fails to disclose or suggest filtering target pixel data subject to filtering using the predetermined pieces of pixel data, thereby outputting filtered pixel data and non-filtered pixel data, the predetermined pieces of the pixel data including the target pixel data subject to filtering and non-target pixel data subject to filtering, wherein the non-filtered pixel data is generated by the non-target pixel data subject to filtering. As a result, the general mention of filtering in combination with the disclosure of the FIFO 10 in Akerib does not disclose or suggest the specifics of the claimed filtering unit. As a result, Akerib fails to disclose or suggest the claimed filtering unit.

The rejection also indicates that the discussion in Akerib of the operation of an array at column 22, lines 35-45 discloses the claimed setting unit that is operable to set a mode signal indicating whether or not the non-filtered pixel data output by the filtering unit is to be fed. However, this section of Akerib discloses the specifics of how the image exchange mode of the FIFO 10 is implemented. In the image exchange mode, an image previously loaded into the FIFO 10 is transferred into the array for subsequent processing, and the previously processed image from the array is transferred to the FIFO 10 for subsequent output. It is apparent that the portion of Akerib relied upon as disclosing the operation of the claimed setting unit actually describes the makeup of the array, which has two different fields to implement the image

exchange mode, a first field for the new image from the FIFO 10 and a second field for the processed image to be output back to the FIFO 10. (See column 22, lines 11-46). This disclosure of the array does not correspond to the setting of a mode signal indicating whether or not non-filtered pixel data is to be fed. As a result, Akerib fails to disclose or suggest the claimed setting unit.

Further, the rejection relies on the discussion of the components of an embodiment of the associative signal processing apparatus of Akerib at column 14, lines 50-67 as disclosing the claimed data output control unit. However, this section of Akerib indicates that the associative signal processing apparatus includes an array 110 of processors (PEs) 114 and that each of the PEs 114 includes a plurality of memory cells 120. There is no disclosure or suggestion in this portion of Akerib of controlling feeding of non-filtered pixel data according to a mode signal. As a result, Akerib fails to disclose or suggest the claimed data output control unit.

In addition to being patentable over Akerib for the reasons set forth above in support of claim 3, claim 7 is also patentable over Akerib, since claim 7 recites that the predetermined width of the separated image data is less than the width of a line of display. Akerib also fails to disclose or suggest this feature of claim 7.

Because of the above-mentioned distinctions, it is believed clear that claims 3-7 are not anticipated by Akerib. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to modify Akerib or to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 3-7. Therefore, it is submitted that claims 3-7 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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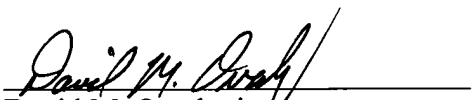
By: 

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December 28, 2007